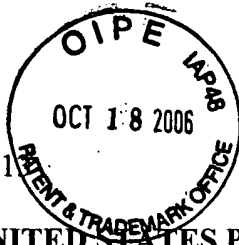


Docket No.: 066365-001



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Simon KNOWLES

Application No.: 10/813,628

Filed: March 31, 2004

Customer Number: 20277

Confirmation Number: 3813

Group Art Unit: 2181

Examiner: LAI, VINCENT

For: APPARATUS AND METHOD FOR CONTROL PROCESSING IN DUAL PATH
PROCESSOR

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

In accordance with 37 CFR 1.17(p), please charge the fee of \$180.00 to Deposit Account No. 500417.

10/19/2006 MBERHE 00000046 500417 10013628
01 FC:1806 180.00 DA

10/813,628

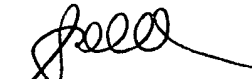
The references **US 5,423,051, US 2005/0044434 A1, and the references by BOLOTSKI, et al. and STOKES** were first cited on the form PTO-892 dated May 22, 2006 of corresponding US Patent Application No. 10/813,615.

The references **US 2002/010852, US 2002/174266, US 6,061,367, US 2002/063577, and the reference by Alippi, et al.** were first cited in an International Search Report of corresponding US Patent Application No. 10/813,433. The reference **US 5,737,631** was first cited on the form PTO-892 dated May 22, 2006 of corresponding US Patent Application No. 10/813,433.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Stephen A. Becker
Registration No. 26,527

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 SAB:jjz
Facsimile: 202.756.8087
Date: October 18, 2006

**Please recognize our Customer No. 20277
as our correspondence address.**



SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)				ATTY. DOCKET NO. 066365-0013		SERIAL NO. 10/813,628	
				APPLICANT Simon KNOWLES			
				FILING DATE March 31, 2004		GROUP 2181	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document		Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		US 5,423,051	06-06-1995	FULLER et al.			
		US 2005/0044434 A1	02-24-2005	KAHLE et al.			
		US 5,737,631	04-07-1998	TRIMBERGER			
		US 2002/0010852 A1	01-24-2002	ARNOLD et al.			
		US 2002/0174266 A1	11-21-2002	PALEM et al.			
		US 6,061,367	05-09-2000	SIEMERS			
		US 2002/0063577 A1	05-30-2002	ABBOTT			
		US					
		US					
		US					
		US					
		US					
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number + -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document		Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
		BOLOTSKI, et al., "Unifying FPGAs and SIMD Arrays," M.I.T. Transit Project, February 8, 1994, pp. 1-22, Transit Note #95.					
		STOKES, "A Brief Look at the PowerPC 970," Ars Technica, 2002, pp. 1-3.					
		ALIPPI, et al., "Determining the Optimum Extended Instruction-Set Architecture for Application Specific Reconfigurable VLIW CPUs," IEEE, 2001, pp. 50-56.					
EXAMINER				DATE CONSIDERED			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.